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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,247	03/31/2004	Jon K. Kriegel	ROC920040010US1	8153

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Robert R. Williams
IBM Corporation, Dept. 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
MISIURA, BRIAN THOMAS	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,247	KRIEGEL, JON K.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1,8-12 and 14* is/are rejected.

7)☒ Claim(s) *2-7,13 and 16-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Objections

Claims 16-21 are objected to because of the following informalities: Claims 16, 17 and 19 are dependent upon Claim 14, however, the examiner believes they were meant to be dependent upon Claim 15 according to their claim language. Claims 16-21 will be treated as though they were dependent upon claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1, 8-10, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker et al. U.S. Patent No. 5,832,279, in view of Hewitt et al. U.S. Patent No. 6,339,808.

Per claim 1, Rostoker discloses:

- an abstraction layer comprising a first plurality of registers conforming to the specific interrupt architecture (Rostoker, column 5 line 66 – column 6 line 6, figures 1 and 2);
- an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors (figure 1 numeral 12), comprising a second plurality of registers which correspond to the first plurality of registers (figure 3, numeral 58), wherein the implementation dependent layer is configured to receive interrupts and forward received interrupts to the one or more processors (Rostoker, column 6 lines 24-31, figures 1-3).

Rostoker does not disclose: to read and write data to the second plurality of registers in response to interrupts processed through the one or more processors.

However, Hewitt discloses to read and write data to the second plurality of registers in response to interrupts processed through the one or more processors (Hewitt, column 7 lines 49-60, figure 2).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Hewitt into the system of Rostoker to provide a system where the registers are utilized in the processing of data during an interrupt process.

- The modification would have been obvious because one having ordinary skill in the art would want to have a system where the registers are utilized in the processing of data during an interrupt process (Hewitt, column 7 lines 49-60, figure 2).

Per claim 8, Rostoker discloses the apparatus of claim 1, wherein the specific interrupt architecture is an Advanced Programmable Interrupt Controller (APIC) architecture

(Rostocker, column 4 line 66 - column 5 line 7, figure 1).

Per claim 9, Rostoker discloses the apparatus of claim 8, wherein the first plurality of registers comprises one or more register sets in full compliance with the APIC architecture (Rostocker, column 5 line 57- column 6 lines 6, figure 1 and 2).

Per claim 10, Rostoker discloses the apparatus of claim 8, wherein the first plurality of registers comprises one or more register sets which provide operational similarity with the APIC architecture (Rostocker, column 5 line 57- column 6 lines 6, figure 1 and 2).

Per claim 12, Rostoker discloses

- providing an abstraction layer comprising a first plurality of registers conforming to the specific interrupt architecture (Rostoker, column 5 line 66 – column 6 line 6, figures 1 and 2);

- providing an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors (figure 1 numeral 12), comprising a second plurality of registers which correspond to the first plurality of registers (figure 3, numeral 58; receiving interrupts and forwarding received interrupts to the one or more processors through the implementation dependent layer (Rostoker, column 5 line 66 – column 6 line 38, figures 1-3);

Rostoker does not disclose: reading and writing data to the second plurality of registers in response to interrupts processed through the one or more processor.

However, Hewitt discloses reading and writing data to the second plurality of registers in response to interrupts processed through the one or more processor (Hewitt, column 7 lines 49-60, figure 2).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Hewitt into the system of Rostoker to provide a system where the registers are utilized in the processing of data during an interrupt process.

- The modification would have been obvious because one having ordinary skill in the art would want to have a system where the registers are utilized in the processing of data during an interrupt process (Hewitt, column 7 lines 49-60, figure 2).

2. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker et al. U.S. Patent No. 5,832,279, in view of Hewitt et al. U.S. Patent No. 6,339,808, in further view of Burgess, U.S. Patent No. 6,892,260.

Per claim 11, Both Rostoker and Hewitt do not disclose the apparatus of claim 8, wherein the one or more processors are PowerPC processors.

However, Burgess discloses the apparatus of claim 8, wherein the one or more processors are PowerPC processors (Burgess, column 2 lines 30-64, figures 1-3).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Burgess into the system of Rostoker and Hewitt to combine the advantages of the claimed system with those of a PowerPC processor.

- The modification would have been obvious because one having ordinary skill in the art would want to combine the advantages of the claimed system with those of a PowerPC processor (Burgess, column 2 lines 30-64, figures 1-3).

Per claim 14, since the limitations of this claim have already been described in this action, please refer to the above rejections for claims 8 and 11.

Allowable Subject Matter

3. Claims 2-7, and 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: claims 15-21 are deemed allowable over the prior art of record as the prior art fails to teach or suggest the following limitations.

1. an abstraction layer comprising a plurality of address decoders and a first plurality of registers conforming to the specific interrupt architecture.

2. the register control logic circuit configured to receive control signals from the register access generator and address decodes from one or more address decoders in the abstraction layer.

However, Claims 16-21 are objected to because of minor informalities as explained above. Once these informalities have been appropriately corrected, these claims will be subject for allowance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTM

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/16/05